Listing of Claims

This listing of claims replaces all prior versions of the claim set.

1. (Canceled).

2. (Previously Presented) A method of forming a semiconductor device comprising:

patterning a metal-gate layer and a gate polysilicon layer to form a gate pattern comprising a gate polysilicon pattern and a metal-gate pattern;

covering sidewalls of the metal-gate pattern with an oxidation barrier layer, wherein the oxidation barrier layer comprises metal; and

forming the oxidation barrier layer on the sidewall of the metal gate pattern using chemical vapor deposition (CVD) or an atomic layer deposition (ALD).

3. (Previously Presented) The method of claim 2, wherein the oxidation barrier layer comprises at least one of an oxide, nitride, or oxynitride of the metal.

4. (Previously Presented) The method of claim 3, wherein the metal comprises at least one of the following: aluminum (Al), tantalum (Ta), titanium (Ti), hafnium (Hf) and gold (Au).

5. (Previously Presented) A method of forming a semiconductor device comprising:

patterning a metal-gate layer and a gate polysilicon layer to form a gate pattern comprising a gate polysilicon pattern and a metal-gate pattern;

covering sidewalls of the metal-gate pattern with an oxidation barrier layer, wherein the oxidation barrier layer comprises metal; and

sequentially forming a gate insulator layer, a gate polysilicon layer and a metal gate layer on a semiconductor substrate prior to the patterning step,

wherein the covering step comprises depositing a metal layer and oxidizing or nitrifying the deposited metal layer.

6. (Previously Presented) A method of forming a semiconductor device comprising:

patterning a metal-gate layer and a gate polysilicon layer to form a gate pattern comprising a gate polysilicon pattern and a metal-gate pattern; and

covering sidewalls of the metal-gate pattern with an oxidation barrier layer, wherein the oxidation barrier layer comprises metal,

wherein the oxidation barrier layer comprises aluminum oxide (Al_2O_3), and wherein the covering step comprises:

forming an aluminum layer using a CVD method by supplying methylpyrrolidine alane (MPA) as a source gas and argon (Ar) of 100sccm as a carrier gas at a temperature of between about 135~145°C and at a pressure of between about 0.1~1.1Torr; and

oxidizing the aluminum layer in an enriched oxygen environment.

7. (Previously Presented) The method of claim 5, wherein the oxidation barrier layer has a thickness of between about 5~100Å.

8. (Previously Presented) A method of forming a semiconductor device comprising:

patterning a metal-gate layer and a gate polysilicon layer to form a gate pattern comprising a gate polysilicon pattern and a metal-gate pattern;

covering sidewalls of the metal-gate pattern with an oxidation barrier layer, wherein the oxidation barrier layer comprises metal; and

forming a barrier metal layer between the metal gate layer and the polysilicon layer, and wherein the gate pattern comprises a stacked gate polysilicon pattern, barrier metal pattern and metal gate pattern.

9. (Original) The method of claim 8, wherein the barrier and/or metal gate layer comprises tungsten.

10.(Previously Presented) The method of claim 8, wherein the barrier metal layer

comprises tungsten nitride (WN) or titanium nitride (TiN).

11. (Previously Presented) The method of claim 8, wherein the oxidation barrier layer is selectively configured to cover substantially only the sidewall(s) of the metal gate layer and the barrier metal layer.

12. (Previously Presented) The method of claim 5, further comprising forming a capping layer on the metal-gate layer, wherein the capping layer is patterned when the metal-gate layer and the gate polysilicon layer are sequentially patterned, thereby forming a stacked gate pattern comprising, in serial order, a gate polysilicon pattern, a metal-gate pattern and a capping pattern.

13. (Previously Presented) The method of claim 5, further comprising forming a spacer layer to substantially cover a sidewall of the gate pattern including about: (a) the sidewall(s) of the polysilicon pattern; (b) sidewall(s) of the oxidation barrier layer over the metal-gate layer; and (c) the sidewall(s) of the capping pattern.

14. (Previously Presented) The method of claim 5, further comprising forming an impurity-doped region in the semiconductor substrate at opposing sides of the gate pattern using the gate pattern as an ion-implantation mask.

15.(Previously Presented) The method of claim 5, further comprising thermally treating the semiconductor substrate having the gate pattern with the oxidation barrier layer under an oxygen-enriched environment.

16. (Previously Presented) The method of claim 15, wherein the thermally treating under the oxygen-enriched environment comprises supplying nitrogen as a carrier gas, oxygen, and hydrogen at a temperature of between about 750~950°C and a ratio of oxygen/hydrogen of between about 0.5~1.3.

17.(Previously Presented) A method of forming a metal gate electrode comprising:

forming a gate pattern comprising a metal-gate pattern on a target substrate;

depositing a metal layer; and

oxidizing or nitrifying the deposited metal layer to form an oxidation barrier layer covering sidewalls of the metal-gate pattern.

18. (Currently Amended) A method according to Claim 17, wherein forming a gate pattern comprises;

forming a polysilicon gate layer and a metal gate layer on the target substrate; and

patterning the metal gate layer and the polysilicon gate layer to form a polysilicon-gate pattern and the metal-gate pattern.

19. (Previously Presented) A method according to Claim 18, wherein the metal gate layer comprises tungsten and the metal layer comprises aluminum, tantatum, titanium, hafnium, and gold.

20. (Previously Presented) A method according to Claim 18, further comprising forming a barrier metal layer between the polysilicon gate layer and the metal gate layer, and further comprising forming a capping layer on the metal gate layer.

21. (Previously Presented) A method according to Claim 17, wherein depositing a metal layer comprises depositing the metal layer using a chemical vapor deposition or an atomic layer deposition.

22. (Previously Presented) A method according to Claim 17, wherein depositing a metal layer comprises depositing an aluminum layer, and wherein oxidizing or nitrifying the deposited metal layer comprises oxidizing the aluminum layer in an enriched oxygen environment.

23. (Previously Presented) A method of forming an integrated circuit device having a metal gate electrode comprising:

forming a stacked gate pattern onto a target substrate, the gate pattern comprising a metal-gate pattern with opposing first and second surfaces and at least one sidewall; and

covering at least a portion of the at least one sidewall of the metal-gate pattern with an oxidation barrier layer substantially without covering a sidewall of an adjacent gate polysilicon layer with the oxidation barrier layer, wherein the oxidation barrier layer comprises aluminum oxide (Al_2O_3), and wherein the covering step comprises:

forming an aluminum layer using a CVD method by supplying methylpyrrolidine alane (MPA) as a source gas and argon (Ar) as a carrier gas at a temperature above ambient; and

oxidizing the aluminum layer in an enriched oxygen environment to provide the oxidation barrier layer.

24. (Original) A method according to Claim 17, further comprising thermally treating the target substrate having the gate pattern with the oxidation barrier layer in an oxygen-enriched environment.

25. (Previously Presented) A method according to Claim 24, wherein the thermally treating under the oxygen-enriched environment comprises supplying nitrogen as a carrier gas, oxygen, and hydrogen at a temperature of between about 750~950°C and a ratio of oxygen/hydrogen of between about 0.5~1.3.

26-27. (Canceled)